REMARKS

Claims 2, 4, 5, 7, 9, 10, 16, 18 and 19 were allowed. Claim 14 was found to be allowable subject matter.

Applicant hereby acknowledges the Examiner's reasons for indication of allowable subject matter. Applicant respectfully notes that there may be additional reasons for indication of allowable subject matter that have not been specifically cited, and which may apply to various of the allowable claims, in addition to or instead of the cited Reasons. Applicant respectfully suggests that notwithstanding the Examiner's reasons for indication of allowable subject matter, it is believed that each of the allowable claims is patentable in its own right and/or for other reasons raised during the prosecution and/or explained in the specification of this application.

To the extent that any statements regarding patentability of any claims allowed by the Examiner made by the Applicant or the Examiner in any document filed in this application are inconsistent with or not included in the Examiner's reasons for indication of allowable subject matter, they are incorporated by reference herein.

Claims 1, 3, 6, 8, 11-13, 15, 17, and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Fujimoto et al., U.S. Patent No. 5,933,050.

Applicant respectfully traverses this rejection. The Applicant respectfully disagrees with the statement of the Examiner that, "Based on the function of these units as disclosed by Applicant, a correlation may be made with the Fujimoto elements that one would have been obvious to one of ordinary skill at the time of Applicant's invention albeit the use of different terminology", (Office Action, page 2, paragraph 3, lines 5-8). The units referred to in the present invention are the inspection item and logical design.

However, the Examiner admits that, "Fujimoto discloses a semiconductor device development integrating system that stores and manages electronic data created in a semiconductor device design process", (emphasis added) (Office Action, page 2, paragraph 3, lines 2-4). In other words, Fujimoto et al. only discloses a system that stores and manages electronic data representing a design; the system does not execute the design itself of the semiconductor device.

In contrast, independent claims 1, 13, and 15 and the dependent claims rejected herein, include the execution of a logical design of a semiconductor integrated circuit.

With regard to the inspection item, as claimed herein in the rejected claims, it is claimed as a necessary reference to the logical design of a semiconductor integrated circuit, such execution of a logical design nowhere being disclosed, taught, or suggested by Fujimoto et al.

The detailed analysis of the Examiner of claims 1, 13, and 15, in the Office Action, does not rebut the above argument.

In regard to claim 1, the Examiner cites Fig. 1, element 102, and Fig. 2b, element 10, in connection with the circuit design unit which executes a logical design of the semiconductor integrated circuit, claimed in claim 1. However, element 102 is a semiconductor device design electronic terminal implemented on an engineering work station (EWS) 10. This terminal or workstation issues a request to the semiconductor device management system 101 to call and display the integrated semiconductor device information and to create and edit design data based on the information. The semiconductor device information management system 101, in turn, stores and manages electronic data on the photomask specifications created in the semiconductor device design process and electronic data on the device manufacture process, (column 6, lines

48-55; column 7, lines 35-42, 45-52). It is clear from this description that element 102, implemented as element 12, does not perform any design. Nor for that matter does system 101. These elements merely use data generated by a semiconductor device design process which is not performed by any of these elements.

In addition, in the rejection of claim 1, the Examiner cites database 3 in connection with the inspection item database section claimed in claim 1, and cites element 104 in Fig. 1 in connection with the description of the inspection database section as containing a circuit feature of said semiconductor integrated circuit corresponding to at least one inspection item of an inspection to be executed before layout design of the semiconductor integrated circuit is executed. Although database 3 can be construed as containing inspection data since it stores information created at an evaluation section, (column 6, lines 26-27), element 104 in Fig. 1 is simply the semiconductor device manufacturing terminal implemented by the EWS 20 in Fig. 2(b), (column 7, lines 60-62). Nothing in the disclosure in Fujimoto et al. links element 104 to layout design of a semiconductor integrated circuit; element 104 is only connected with the manufacture of a semiconductor device.

In support of the rejection of claim 15, the Examiner cites the same elements of Fujimoto et al. discussed above in connection with claim 1.

With regard to claim 13, the Examiner cites column 6, lines 4-7, in support of the presence in Fujimoto et al. of an inspection item database section, in which a circuit feature of a semiconductor integrated circuit for which a logical design should be executed, corresponds to an inspection item of an inspection to be executed before a layout design of the semiconductor integrated circuit is executed. However, column 6, lines 4-7, is merely a short description of Fig.

14, and appears to have nothing to do with an inspection item database section. With regard to the provision in claim 13 of executing the logical design of the semiconductor integrated circuit by the circuit designer with reference to the notified inspection item, the Examiner cites column 7, lines 56-65. However, column 7, lines 56-65, only refers to the manufacture of a semiconductor device, not its design.

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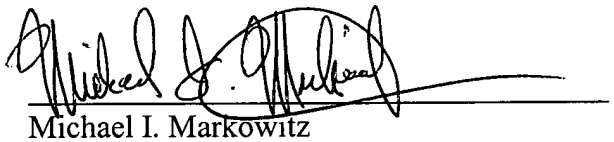
Respectfully submitted,



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